

Defects in nitride semiconductors: From nanoscale imaging to macroscopic device behavior

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Abstract

Scanning capacitance microscopy (SCM), atomic force microscopy (AFM), and conductive AFM are used to image the spatial distribution and electronic properties of threading dislocations in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ epitaxial layers grown by molecular-beam epitaxy. SCM imaging reveals that GaN growth directly on SiC substrates leads to clustering of negatively charged dislocations at nucleation island boundaries, while incorporation of an AlN buffer leads to a random spatial distribution of negatively charged dislocations. Numerical simulations demonstrate that clustered dislocations are less effective in depleting mobile carriers. AFM and conductive AFM imaging reveal the presence of highly conductive threading dislocations which lead to excessive reverse-bias leakage current flow in Schottky diodes. Temperature-dependent current–voltage spectroscopy is used to develop a model for current flow via these dislocations based on a Frenkel–Poole emission process. On the basis of this model, heterostructures are designed to suppress this emission mechanism. Conductive AFM imaging and electrical measurements then confirm the expected suppression of leakage current and specifically of the Frenkel–Poole emission process, demonstrating the validity of both the proposed mechanism of current flow and the approach for leakage current suppression.

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1. Introduction

Group III-nitride semiconductors have been a subject of intense interest and research activity for both electronic [1–3] and optoelectronic [4,5] device applications. However, the lack of a suitable substrate for homoepitaxial growth typically leads to high concentrations of defects, particularly

dislocations, in epitaxial nitride films. Because threading dislocations in nitride semiconductors often exhibit prominent electrical behavior, including large negative charge densities in the dislocation core [6,7] and, in material grown by molecular-beam epitaxy (MBE), high conductivity, [8–10] characterization and understanding of the electrical properties of defects and material inhomogeneities plays an essential role in the science and engineering of nitride semiconductor materials and devices.

Here we characterize the presence, spatial distribution, and electrical behavior of dislocations in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterostructure field-effect transistor (HFET) epitaxial layer structures using

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scanning probe microscopy. The ability to image both surface structural morphology and either surface or near-surface electrical characteristics at the nanoscale enables the correlation of various electrical behaviors, such as charge modulation or conductivity, with the presence of individual defects identified via their manifestation in surface morphology. These studies are then combined with macroscopic electrical device characterization and numerical simulations to correlate the presence and properties of individual defects with the electrical behavior of macroscopic devices, and on the basis of the resulting understanding to design nitride semiconductor heterostructures in which key undesirable aspects of defect electrical behavior are mitigated.

2. Experimental methods

$\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HFET structures were grown by MBE on semi-insulating on-axis 4H-SiC substrates. The epitaxial layer structures consisted of a 25 nm $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer with $x = 0.25\text{--}0.26$ grown on a 1.3–3 μm GaN film at 720–750 °C under slightly metal-rich conditions. All layers were nominally undoped. To determine the effects of a high-temperature (800 °C) AlN buffer layer on the properties of subsequently grown material, a pair of samples were grown under nominally identical conditions with and without a ~ 60 nm AlN buffer layer deposited on the SiC substrate. For electrical studies of Schottky diode leakage current characteristics, Ti/Al metallization annealed at 800 °C for 3 min was used to form Ohmic contact rings, within which 125 μm -diameter Ni dots were used to form Schottky contacts. Current–voltage characteristics were measured at temperatures ranging from 110 to 400 K.

Scanning capacitance microscopy (SCM) was carried out in a Digital Instruments Dimension 3100 microscope with W_2C -coated probe tips. Local conductivity measurements were carried out by conductive atomic force microscopy [11] (AFM) in a modified Digital Instruments Nanoscope[®] IIIa MultiModeTM microscope under ambient atmospheric conditions (~ 20 °C with 50% relative humidity) using highly doped diamond-coated probe tips. Two- and three-dimensional numerical simulation of material and device characteristics was carried out using Silvaco simulation software.

3. Analysis of spatial distribution of negatively charged dislocations

3.1. Experimental results

The presence and spatial distribution of negatively charged dislocations are revealed through local depletion, and accompanying capacitance shifts, that are imaged with SCM [12–14]. Representative SCM images of $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HFET epitaxial layer structures grown with and without AlN buffer layers are shown in Fig. 1, in which regions depleted by charged dislocations appear bright [15]. Images of the sample grown with no buffer layer, shown in Figs. 1(a) and (b), exhibit a domain-like microstructure with negatively charged dislocations grouped at boundaries between 2 and 4- μm diameter domains. This columnar microstructure is commonly observed in GaN-based materials [16–18] and is a result of discrete island nucleation followed by island expansion and coalescence with dislocations forming at island boundaries to accommodate island orientation mismatch. SCM images of the sample grown with the AlN buffer, shown in Figs. 1(c) and (d), reveal an apparently random dislocation distribution, most likely arising from the relatively small lattice mismatch ($\sim 1\%$) between AlN and SiC, which results in two-dimensional pseudomorphic, rather than island, nucleation. By comparing the smaller scan areas

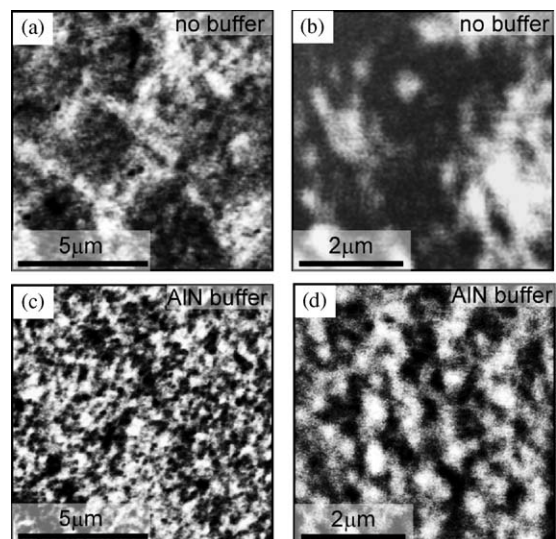


Fig. 1. (a) SCM images of (a) and (b) HFET structure with no AlN buffer layer, exhibiting dislocations at nucleation island domain boundaries, and (c) and (d) HFET structure with a ~ 60 nm AlN buffer, exhibiting randomly distributed dislocations.

shown in Figs. 1(b) and (d), it may be seen that, in general, dislocations reside in groups for the sample grown with no buffer layer and are more uniformly distributed for the sample employing the AlN buffer.

3.2. Numerical simulations

Numerical simulations were used to investigate the dependence of carrier depletion on dislocation spatial arrangement. A schematic diagram of the structure used to model dislocation-induced depletion in an HFET is shown in Fig. 2(a). HFET model parameters, such as bulk carrier density ($\sim 5.5 \times 10^{16} \text{ cm}^{-3}$) and $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier thickness (25 nm) and composition ($x = 0.26$), were assigned values corresponding to the actual samples under investigation. Fixed polarization charges were placed at the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$ interface and top $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ surface, with magnitude chosen to yield the measured electron density at the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$ interface. Simulations of carrier depletion in the bulk employed a similar structure with the $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}$ layer, and associated polar-

ization charges, removed. Fig. 2(b) shows a plot of the simulated band diagram and carrier profile of the HFET structure.

Acceptor states in the dislocation core result in trapped negative charge, locally decreased electrostatic potential, and an accompanying cylindrical depletion region [19]. Fig. 3 shows the electrostatic potential map, extracted from numerical simulations, of a cross-sectional slice through a dislocation in the HFET structure. The potential associated with the dislocation decays much more rapidly near the two-dimensional electron gas (2DEG) channel than in the bulk GaN. The high density of acceptor defect states in the dislocation trap conduction electrons, causing a pronounced upward band bending, and effectively pin the Fermi level near the acceptor energy level. The dislocation charge is screened over a much smaller distance in the 2DEG ($\sim 5 \text{ nm}$) than in the bulk ($\sim 50 \text{ nm}$), due to the extremely high charge density in the 2DEG.

The substantial extent of the depleted region in the vicinity of a single dislocation suggests that dislocation charge and carrier depletion effects may depend, to a significant degree, on the distance between dislocations. To study such depletion effects in the bulk, four dislocations were included in bulk GaN and their separations varied. In prior studies, dislocation arrays have been observed with typical inter-dislocation spacings of 5–100 nm [20,21] and high-quality GaN deposited by plasma assisted MBE on SiC has been found to exhibit dislocation densities from $\sim 10^8$ to $\sim 10^{10} \text{ cm}^{-2}$. Therefore, dislocation separations of 10, 20, 40, 80, and 160 nm have been examined and the simulation area has been scaled to achieve effective

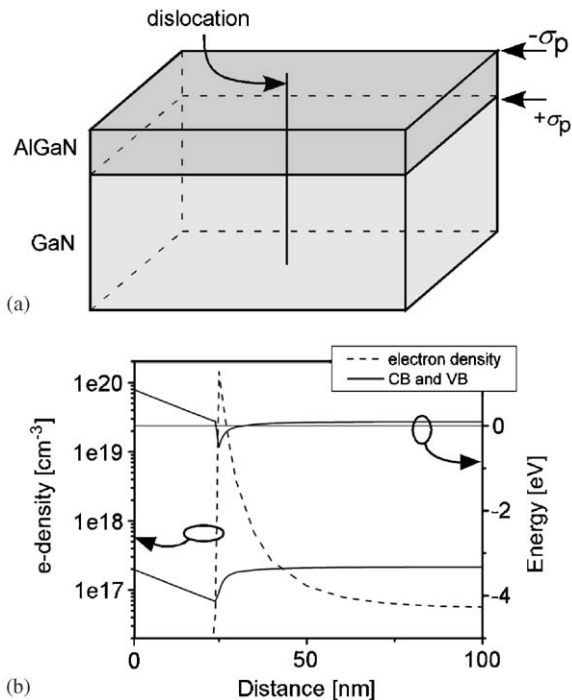


Fig. 2. (a) Schematic diagram of simulated $\text{Al}_{0.26}\text{Ga}_{0.74}\text{N}/\text{GaN}$ HFET structure, and (b) resulting band-edge energy diagram and carrier distribution.

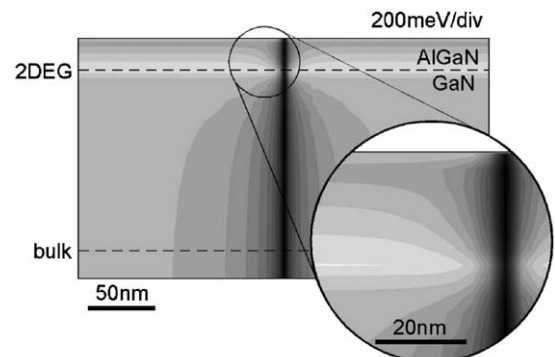


Fig. 3. Cross-sectional view of electrostatic potential of a single charged dislocation, showing reduction in extent of depletion region near 2DEG.

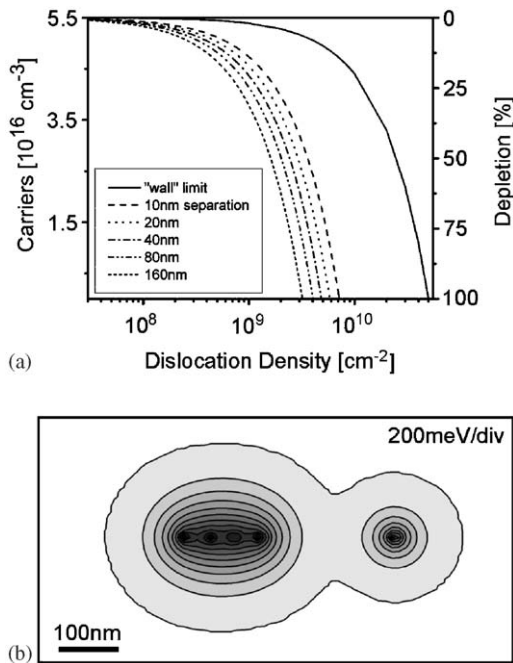


Fig. 4. (a) Carrier density in bulk GaN with 4 dislocations in a simulation area normalized for equivalent dislocation densities of 10^7 to 10^{10} cm⁻² with inter-dislocation separations varied from 10 to 160 nm. Depletion approximation solution for lower limit of dislocation separation (labeled “wall” limit) is plotted as a solid line. (b) Plot of electrostatic potential for 4 closely spaced dislocations and a single isolated dislocation, demonstrating lateral broadening of potential distribution for closely spaced dislocations.

dislocation densities from 10^7 to 10^{10} cm⁻². Fig. 4(a) shows the resulting bulk-free carrier densities and percentage of carriers depleted. These results indicate that increased dislocation spacing results in more efficient carrier depletion and a reduced free carrier density, and demonstrate the pronounced effect that dislocation arrangement can have on free carrier density.

The lower limit of dislocation spacing is also treated analytically, using the one-dimensional depletion approximation for a potential barrier $\Delta\phi \approx E_F - E_T$ and assuming a dislocation “wall” with an inter-dislocation separation of 5 nm [20]. This case is included in the plot of Fig. 4(a) as the solid line. From the predicted carrier densities plotted in Fig. 4(a), it may be seen that at a dislocation density of 2×10^9 cm⁻², the expected free carrier concentration can vary from 2 to 4×10^{16} cm⁻³, based purely on dislocation arrangement; at a dislocation density of 3×10^9 cm⁻², there may be a factor of 8 higher density of free carriers

for materials with closely spaced dislocations. Based on these results, it is clear that the spatial distribution of charged dislocations can have a significant effect on the resulting free carrier density.

Effects of dislocation interaction on the electrostatic potential distribution are further illustrated in Fig. 4(b). Here, 4 dislocations are placed at 40 nm separation with a single dislocation located 220 nm away from this group. As individual depletion regions overlap, the depletion extends in the transverse direction. This results in a wider depletion region and corresponds to the spatially broader features seen in Figs. 1(a) and (b) (600–1200 nm) for the sample that exhibited grouped dislocations compared to those in Figs. 1(c) and (d) (300–600 nm) corresponding to uniformly distributed dislocations. These observed feature sizes are larger than the potential features predicted from our simulations, most likely due to convolution of the actual feature with the tip size and the lateral spread of the induced depletion region under the reverse bias conditions used [22].

4. Analysis of leakage currents induced by conductive dislocations

4.1. AlGa_xN/GaN epitaxial layer structures

Conductive screw dislocations have been established as the primary source of room-temperature reverse-bias leakage current in Schottky diodes fabricated from nitride epitaxial layers grown by MBE under metal-rich conditions [8–10]. However, the detailed mechanisms giving rise to and governing this current flow have not been well established. To address this issue, we performed both nanoscale imaging of current flow in Al_xGa_{1-x}N/GaN HFET epitaxial layer structures, to confirm the presence and assess the properties of conductive screw dislocations in these structures, and temperature-dependent current–voltage spectroscopy on Schottky diodes, to analyze the physical mechanisms governing leakage current flow.

Fig. 5 shows topographic and current images, obtained by conductive AFM with a sample bias of +12 V, of an Al_{0.25}Ga_{0.75}N/GaN HFET structure. Conductive dislocations (dark spots in the conductive AFM images) are clearly evident, at a density of $\sim 1 \times 10^9$ cm⁻², confirming that these dislocations dominate leakage current flow at room temperature. Fig. 6 shows current density as a function of bias voltage for a Schottky diode fabricated from the

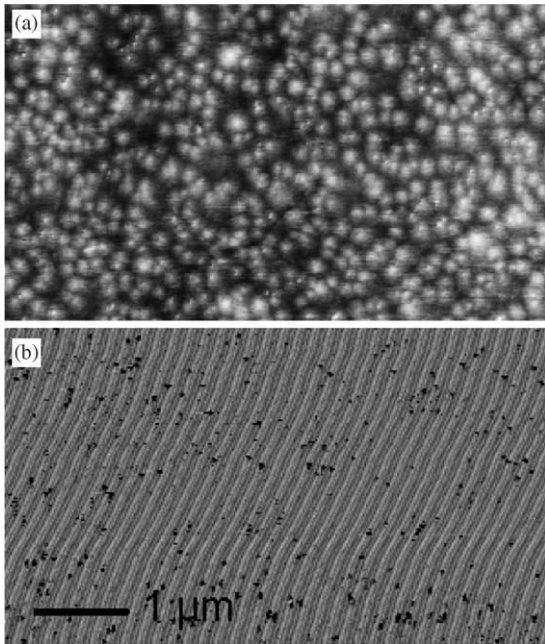


Fig. 5. (a) Topographic image and (b) current image obtained with +12 V bias applied to the sample of $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ HFET epitaxial layer structure, showing localized current flow (dark spots in current image) associated with pure screw dislocations.

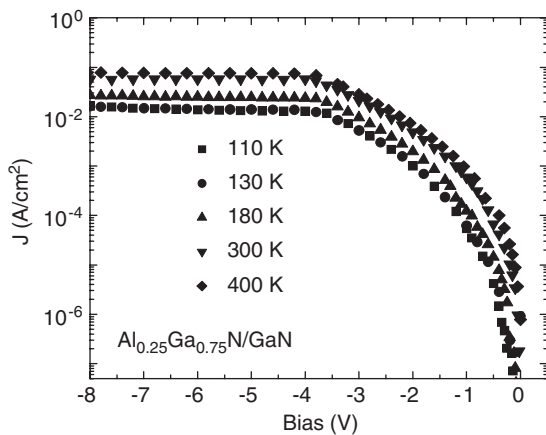


Fig. 6. Reverse-bias Schottky diode current density for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ HFET structure, for temperatures from 110 to 400 K.

same $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}/\text{GaN}$ HFET structure. At temperatures below ~ 150 K, the reverse-bias leakage current is nearly independent of temperature, suggesting that tunneling is the dominant source of current flow. A detailed analysis [23] confirms that a Fowler–Nordheim model for tunneling current provides a good quantitative description of

the measured current density in this temperature range.

For temperatures above 250 K—the temperature regime for which we expect conductive dislocations to dominate reverse-bias leakage current—the measured Schottky diode current densities are observed to be dependent on both electric field and temperature. A detailed analysis [23] reveals that, upon quantitative consideration of numerous possible models for current transport, only a transport model based on Frenkel–Poole emission describes all the data with good quantitative accuracy while yielding realistic values for the necessary physical parameters. Frenkel–Poole emission refers to electric-field-enhanced thermal emission from a trap state into a continuum of electronic states—usually, but not necessarily, the conduction band in an insulator. The current density associated with this mechanism is given by [24–26]

$$J = CE_b \exp \left[-\frac{q(\phi_t - \sqrt{qE_b/\pi\epsilon_0\epsilon_s})}{kT} \right], \quad (1)$$

where E_b is the electric field in the semiconductor barrier at the metal–semiconductor interface, ϕ_t is the barrier height for electron emission from the trap state, ϵ_s is the relative dielectric permittivity at high frequency, T is temperature, ϵ_0 is the permittivity of free space, and k is Boltzmann’s constant. Our analysis yielded ϵ_s for $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ of 5.1 ± 1.0 , in good agreement with reported values [27,28] of 5.35 for GaN and 4.77 for AlN. ϕ_t obtained from these studies was 0.30 ± 0.03 V, which we interpret in Ref. [23] to be an activation energy for electrons to be excited from a near-surface trap in $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ to a continuum of conductive dislocation states.

4.2. GaN/AlGaIn/GaN epitaxial layer structures

The strong dependence of Frenkel–Poole emission on semiconductor electric field immediately suggests a strategy for suppression of this transport mechanism. Polarization charges present at $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ heterojunction interfaces enable reversal of the electric field at the metal–semiconductor interface in an HFET structure by incorporation of a thin GaN layer atop the conventional $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier, as shown in Fig. 7. In epitaxial layer structures grown by metalorganic chemical vapor deposition (MOCVD), this has been shown to yield a large reduction in

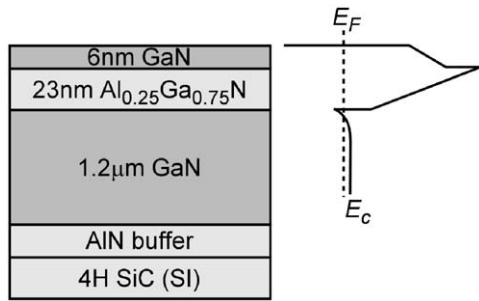


Fig. 7. Schematic band-edge energy diagram for GaN/ $\text{Al}_x\text{Ga}_{1-x}\text{N}$ /GaN HFET structure incorporating a GaN cap layer atop the conventional $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier.

Schottky diode leakage current density due to the increase in barrier height resulting from the negative polarization charge at the upper GaN/ $\text{Al}_x\text{Ga}_{1-x}\text{N}$ interface [29].

In material grown by MBE the strategy of increasing the peak barrier height is unlikely to be effective, as current flow is less strongly influenced by Schottky barrier height. However, an additional effect of the insertion of the GaN layer into this structure is a change in the direction of the electric field at the semiconductor surface compared to that in a conventional $\text{Al}_x\text{Ga}_{1-x}\text{N}$ /GaN HFET structure. From Eq. (1) it is evident that the current depends strongly on the electric field at the semiconductor surface, and should be strongly suppressed if the electric field is small, or points from the metal–semiconductor interface into the semiconductor at a Schottky contact.

Fig. 8 shows topographic and current images, at several different bias voltages, obtained by conductive AFM for the conventional $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ /GaN HFET structure and for the structure shown in Fig. 7. While current flow in both structures is dominated by localized conduction associated with dislocations, most evidently at large reverse bias voltages, dislocation-related conduction is strongly suppressed, at a given bias voltage, in the GaN-capped structure compared to that in the conventional HFET. Fig. 9 shows reverse-bias current–voltage characteristics for Schottky diodes fabricated from a GaN-capped HFET structure at temperatures ranging from 250 to 400 K. Comparing these data to the current–voltage characteristics for the conventional $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ /GaN HFET structure shown in Fig. 6, we see that at 300 K, the reverse-bias leakage currents are reduced by one to three orders of magnitude, depending on the bias voltage,

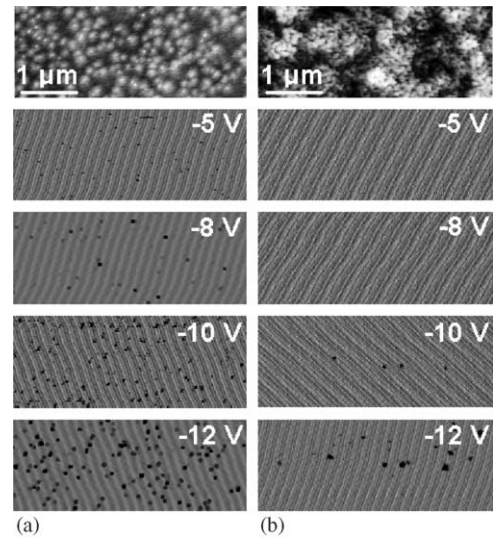


Fig. 8. Topographic and current images for (a) conventional $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ /GaN HFET structure and (b) GaN/ $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ /GaN HFET structure at bias voltages ranging from x to y , showing suppression of dislocation-related leakage current in sample with GaN capping layer.

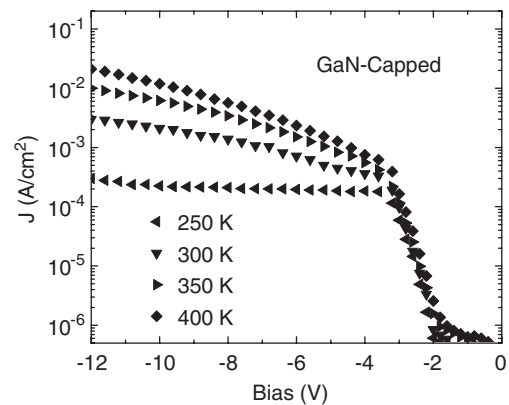


Fig. 9. Reverse-bias Schottky diode current density for GaN/ $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ /GaN HFET structure, for temperatures ranging from 250 to 400 K. The current densities are dramatically reduced compared to those in the conventional HFET structure.

in the GaN-capped HFET structure; the reduction is most pronounced at bias voltages of 0 to -4 V.

Numerical simulations [30] have shown that the direction of the electric field at the metal–semiconductor interface in the GaN-capped structure is inverted compared to that in the conventional HFET structure for bias voltages of 0 to -4 V. For larger reverse bias voltages, the polarity of the electric field at the metal–semiconductor interface is

the same in both structures, but approximately an order of magnitude smaller in the GaN-capped structure. This is expected to lead to a strong, but bias-dependent, suppression in reverse-bias leakage current in Schottky diodes fabricated from the GaN-capped epitaxial layer structure—as is observed experimentally. Furthermore, a thorough quantitative analysis [30] of the leakage currents at large reverse bias voltages in the GaN-capped structure confirms that the current density is well described using the Frenkel–Poole emission model of Eq. (1), provided that the dielectric function and barrier height for GaN— $\epsilon_s = 5.4 \pm 0.1$ and $\phi_t = 0.33 \pm 0.01$ V [23]—are used, as expected since the top layer is GaN rather than $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$. The quantitative agreement between experiment and the Frenkel–Poole emission model at large reverse bias voltages combined with the direct observation of suppressed dislocation-related leakage current by conductive AFM provide strong confirmation that the approach to leakage current suppression described here is valid and highly effective, and can serve on a more general basis as a component of heterostructure design for devices fabricated from MBE-grown nitride material.

5. Conclusions

In summary, we have used a variety of scanning probe techniques to image the nanoscale spatial distribution of dislocations in nitride semiconductor epitaxial layer structures, and to assess the electrical properties of individual dislocations. Motivated by the observation of either clustered or randomly distributed negatively charged dislocations in $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HFET epitaxial layer structures, depending on nucleation and growth conditions, a simulation study was performed which demonstrated that the spatial arrangement of such dislocations can substantially affect their ability to deplete mobile carriers, with dislocation clusters being less effective in doing so. The observation of highly conductive dislocations combined with an analysis of temperature-dependent current–voltage characteristics in Schottky contacts to $\text{Al}_x\text{Ga}_{1-x}\text{N}/\text{GaN}$ HFET structures has enabled the development of a model for reverse-bias leakage current flow based on Frenkel–Poole emission, and demonstration of a highly effective strategy for design of heterostructures in which leakage current flow is suppressed.

Acknowledgments

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