Charging effects in AlGaN/GaN heterostructures probed using scanning capacitance microscopy

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Charging effects in an $Al_xGa_{1-x}N$/GaN heterostructure field-effect transistor epitaxial layer structure have been studied using scanning capacitance microscopy. Voltages of $\leqslant 6$ V applied between an $Al_xGa_{1-x}N$/GaN sample structure and a conducting proximal probe tip are found to create trapped charge in both doped and undoped heterostructures. Scanning capacitance measurements obtained over a wide range of bias voltages allow the charge distribution to be mapped both laterally and in depth with submicron to nanometer scale spatial resolution. Scanning capacitance imaging as a function of bias voltage performed in conjunction with numerical capacitance–voltage simulations suggests that positive charge can be trapped at the $Al_xGa_{1-x}N$ surface and within the GaN layer and negative charge can be trapped at or near the $Al_xGa_{1-x}N$/GaN interface. © *2000 American Vacuum Society.* [S0734-211X(00)00604-1]

I. INTRODUCTION

III–V nitride heterostructures have attracted intense research interest for a variety of device applications including blue light-emitting diodes and lasers,[1] visible-blind ultraviolet photodetectors,[2,3] and high-temperature/high-power electronic devices.[4–9] Although very impressive performance has been demonstrated in many such nitride-based devices, the epitaxially grown nitride materials from which device structures are fabricated typically contain high densities of extended defects such as threading dislocations as well as substantial concentrations of point defects, associated with both of which can be trap states, piezoelectric fields, and other localized variations in electronic structure. These local variations in electronic properties can exert a pronounced influence on device behavior and consequently must be characterized, understood, and controlled in nitride heterostructure materials and device engineering.

In this article, we present studies of local charging of trap states in $Al_xGa_{1-x}N$/GaN heterostructure field-effect transistor (HFET) epitaxial layer structures using scanning capacitance microscopy (SCM). The SCM technique has been applied recently to the characterization of local surface electronic structure in *n*-GaN epitaxial layers[10] and of local variations in threshold voltage in $Al_xGa_{1-x}N$/GaN HFET epitaxial layers.[11] By measuring capacitance properties between a conducting proximal probe tip and the sample structure of interest at a fixed tip-sample bias voltage, lateral variations in mobile carrier distributions, fixed electrostatic or trapped charge distributions, and the resulting local potential distributions can be observed at length scales ranging from <0.1 μm to several μm. Measurement and analysis of SCM image contrast as a function of applied bias voltage then enables such variations to be correlated with various features in structural morphology or with the presence of electrostatic or trapped charge concentrated in specific locations within the sample structure. In this manner we have observed and analyzed, in the studies reported here, localized charging of trap states within $Al_xGa_{1-x}N$/GaN HFET epitaxial layer structures induced by bias voltages applied via a proximal probe tip.

II. EXPERIMENT

The sample structures used in this study, shown schematically in Fig. 1, were grown by metalorganic chemical vapor deposition (MOCVD) on *n*-type 4H-SiC (0001) substrates. For all samples a 0.1 μm AlN buffer layer was initially deposited, followed by an undoped 1.2 μm GaN channel layer and finally the $Al_xGa_{1-x}N$ barrier layer structure. Epitaxial layer structures containing both doped and undoped $Al_xGa_{1-x}N$ layers have been characterized. The barrier layer in the undoped sample consisted simply of 230 Å nominally undoped $Al_{0.15}Ga_{0.85}N$. The barrier layer in the intentionally doped sample, used for the majority of the work described here, consisted of an undoped 30 Å $Al_{0.26}Ga_{0.74}N$ spacer layer followed by a 200 Å *n*-$Al_{0.26}Ga_{0.74}N$ layer doped with Si at a concentration of $3\times10^{18}\,cm^{-3}$. Even in the absence of intentional doping, the polarization fields in the strained $Al_xGa_{1-x}N$ layer will create a two-dimensional electron gas (2DEG) at the $Al_xGa_{1-x}N$/GaN interface.[12–15] The sheet carrier concentrations for these samples, determined from Hall measurements performed at room temperature, were $4.6\times10^{12}\,cm^{-2}$ for the undoped $Al_{0.15}Ga_{0.85}N$/GaN structure and $1.2\times10^{13}\,cm^{-2}$ for the doped $Al_{0.26}Ga_{0.74}N$/GaN structure.

Scanning capacitance microscopy was performed using a Digital Instruments Dimension 3100 atomic force micro-

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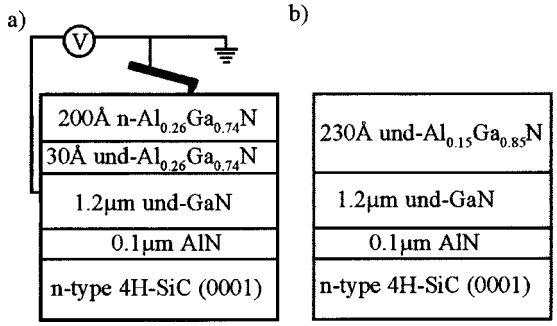

FIG. 1. Schematic diagrams of (a) doped and (b) undoped $Al_xGa_{1-x}N$/GaN HFET epitaxial layer structures. Sample and probe tip geometry and electrical connections are indicated schematically in (a).

scope with a capacitance attachment. The ac and dc bias voltages employed during the scanning capacitance measurements were applied to the sample as indicated in Fig. 1(a). Electrical contact to the epitaxial layers was made using a conducting silver tape contact to the $Al_xGa_{1-x}N$ surface. Previous experiments have shown that there is no measurable difference between contacting the $Al_xGa_{1-x}N$ surface in this manner and contacting the GaN layer through a fully processed ohmic contact. The probe tips used in the measurements presented here were commercially available tips (Digital Instruments) fabricated from highly doped Si. In preparation for imaging, each probe tip assembly was heated at ~250 °C for 30 min to increase the thickness of the native oxide and thereby provide an insulating barrier to minimize current flow between the sample and tip during the SCM measurement. Prior to heating the probe tip and cantilever structure, the underside of the probe substrate was covered with silver paint to ensure that a good electrical contact could be made between the SCM electronics and the tip.

III. RESULTS AND DISCUSSION

Studies of phenomena such as persistent photoconductivity and of trap states in GaN, $Al_xGa_{1-x}N$, and $Al_xGa_{1-x}N$/GaN heterostructures have revealed that epitaxially grown nitride materials are typically characterized by significant densities of defects and impurities, associated with which are a variety of trap states. Filling or emptying, and consequently charging, of deep trap levels during application of large bias voltages in diodes, transistors, and other device structures can then lead to significant transient effects and frequency-dependent device characteristics. These effects can be studied on a spatially localized basis by using the conducting proximal probe tip in the SCM apparatus to apply large, localized bias voltages and observing the subsequent localized charge distribution by SCM imaging and spectroscopy.

In the studies presented here, localized regions of the sample were charged by performing a SCM imaging measurement with a relatively large dc bias voltage (typically $\geq$6 V) applied in conjunction with an ac bias voltage with a typical amplitude of ~2 V. Application of a large bias voltage via the proximal probe tip is roughly analogous to the

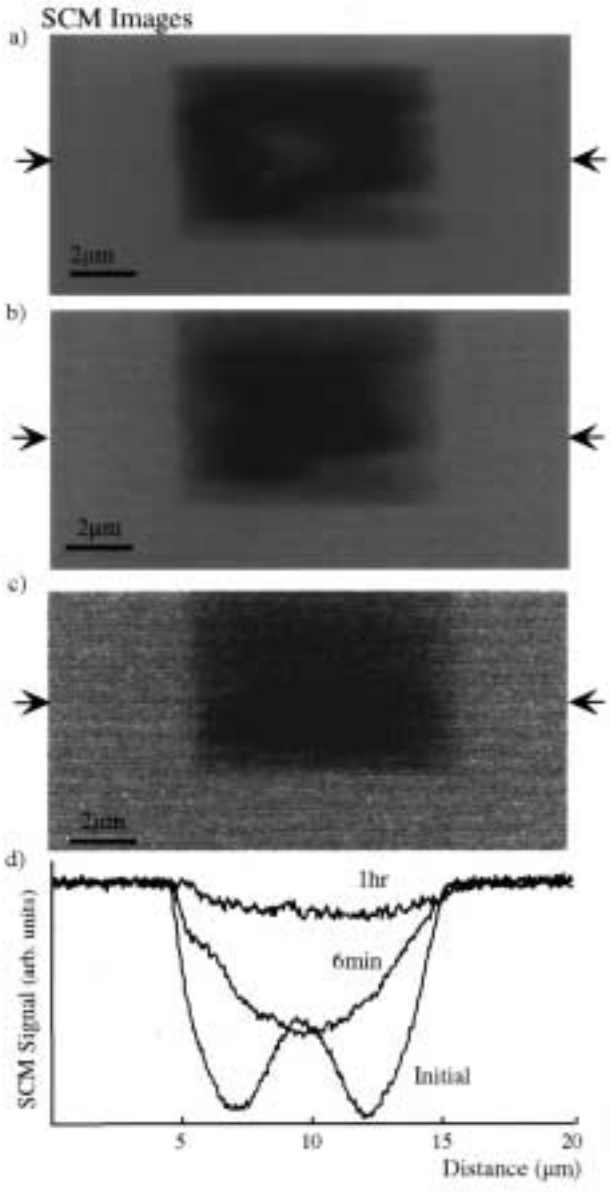

FIG. 2. SCM images obtained at 0 V dc sample bias of a locally charged region of the doped $Al_xGa_{1-x}N$/GaN HFET epitaxial layer structure and surrounding uncharged regions, obtained (a) immediately, (b) 6 min, and (c) 1 h after charging. (d) Line scans extracted from the images (a)–(c) at the locations indicated by arrows.

application of a corresponding bias voltage in a Schottky diode structure. Typically two or more images are obtained under these conditions, after which the scan size is increased and the dc bias voltage reduced to image the charged area along with a surrounding, uncharged region. Figure 2(a) shows a SCM image, obtained at a dc bias of 0 V, of a typical charged region and the surrounding, uncharged area in the undoped $Al_{0.15}Ga_{0.85}N$/GaN HFET structure immediately after charging as described above at a dc sample bias of 6 V. The 0 V dc bias voltage and accompanying ac modulation signal applied during imaging have only a minimal effect on the electrostatic and trapped charge distribution in the sample over the time scales probed in these studies. Figures

2(b) and 2(c) show SCM images of the same charged region shown in Fig. 2(a) obtained 6 min and 1 h after charging, respectively. A minor point to note is that a bright region is present at the center of the image in Fig. 2(a). This contrast disappears within the time (6 min) required to acquire each SCM image, and its origin is currently a subject of investigation.

Figure 2(d) shows line profiles extracted from the images shown in Figs. 2(a)–2(c). The reduction in contrast between the charged and uncharged regions with time, indicative of gradual dissipation of the trapped charge induced by the initial localized application of a large bias voltage, is clearly evident. We have confirmed that this dissipation is not induced by the SCM imaging performed after the initial charging process. The average widths of the charged regions determined from the line profiles (10.43, 10.51, and 10.94 μm for the images obtained immediately, 6 min, and 1 h after the initial charging, respectively) are consistent with a slight lateral spreading of the charge. However, it should be noted that the change in apparent size of the charged region is small compared to the total charged area (less than 1%) and that thermal drift between scans makes it difficult to obtain and compare profiles from identical locations. It should be noted that exposure to UV light removed all indication of charging.

The effects of trapped charge within III–V nitrides have been studied quite extensively. Several groups have reported persistent photoconductivity effects in GaN[16,17] and $Al_xGa_{1-x}N$/GaN heterostructures,[18,19] with the effects observed in $Al_xGa_{1-x}N$/GaN heterostructures being attributed to traps within the $Al_xGa_{1-x}N$ barrier layer in HFET structures.[18] Current collapse in GaN metal-semiconductor field-effect transistors (MESFETs) has been observed and attributed to the presence of trap states within the semi-insulating GaN layer.[20,21] In general, the locations of trap states observed in such studies are inferred based on the electrical behavior of the traps. SCM imaging performed as a function of dc bias voltage allows charge, potential, and mobile carrier distributions to be probed in three dimensions, i.e., with spatial resolution at the submicron to nanometer scale both laterally and in depth. These capabilities provide a unique and powerful method for probing the physical location of trapped charge within an $Al_xGa_{1-x}N$/GaN HFET epitaxial layer structure.

For this purpose, the doped $Al_{0.26}Ga_{0.74}N$/GaN sample, shown schematically in Fig. 1(a), was charged in the manner described above by scanning at a dc bias of 9 V. Following this process, single 10 μm line scans were acquired for dc bias voltages ranging from 0 to 10 V. Line scans for an entire series of voltages spanning this range were acquired within a few minutes of charging, thereby minimizing charge dissipation effects as well as any variations arising from tip wear or changes in environmental factors such as humidity.

Figure 3 shows a series of these line scans for a 2.5 μm charged area in the center of a 10 μm scan line. The dc bias voltage for each scan is indicated in the figure. The SCM signal is plotted in arbitrary units that remain constant for all

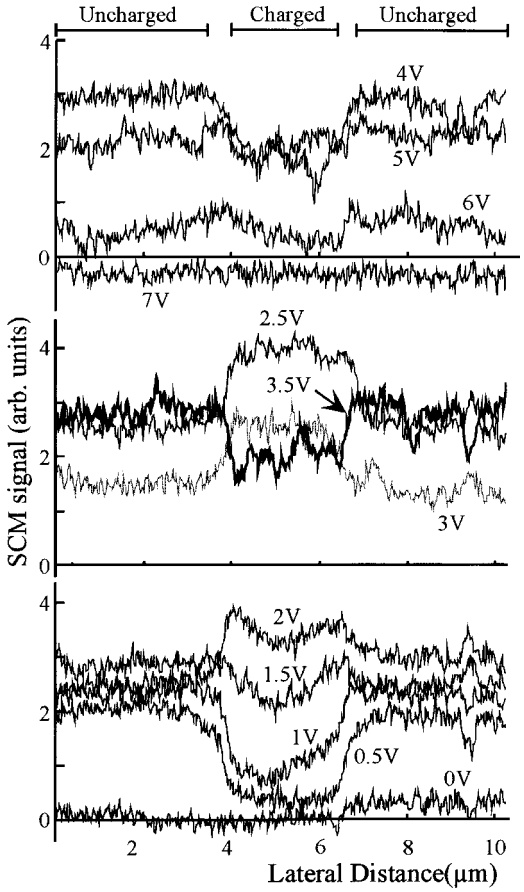

FIG. 3. SCM line scans across a 10 μm×2.5 μm sample region charged at 9 V sample bias, obtained at imaging bias voltages ranging from 0 to 7 V. Bias voltages employed during SCM imaging as well as charged and uncharged regions for all line scans are indicated.

scans. There are two important aspects to consider of the observed dependence of the SCM signal on dc bias voltage: the dependence of the absolute value of the SCM signal on bias voltage, and the contrast between the charged and uncharged regions. At the extremes of the dc bias voltage range illustrated here—<0 V and >7 V—the SCM signal shows little or no contrast between the charged and uncharged regions and the absolute value of the signal is nearly zero. In both the charged and uncharged regions, the absolute value of the SCM signal increases continuously as the dc sample bias voltage is increased from 0 V to ~2.5 V, then decreases substantially at ~3 V. Above 5 V, the signal strength in both regions decreases continuously to nearly zero as the voltage is increased. This general behavior is consistent with that previously observed in SCM studies of $Al_xGa_{1-x}N$/GaN HFET epitaxial layer structures.[11,22]

Figure 4(a) shows a plot of the SCM signal as a function of bias voltage, averaged across the uncharged (dashed line) and charged (solid line) regions within the line scans shown in Fig. 3. At sample bias voltages below 1 V, the SCM signal is larger in the uncharged region than in the charged region. As the dc bias voltage is increased to values above 1.5 V, the contrast between the charged and uncharged regions inverts, with the SCM signal from the charged region remaining

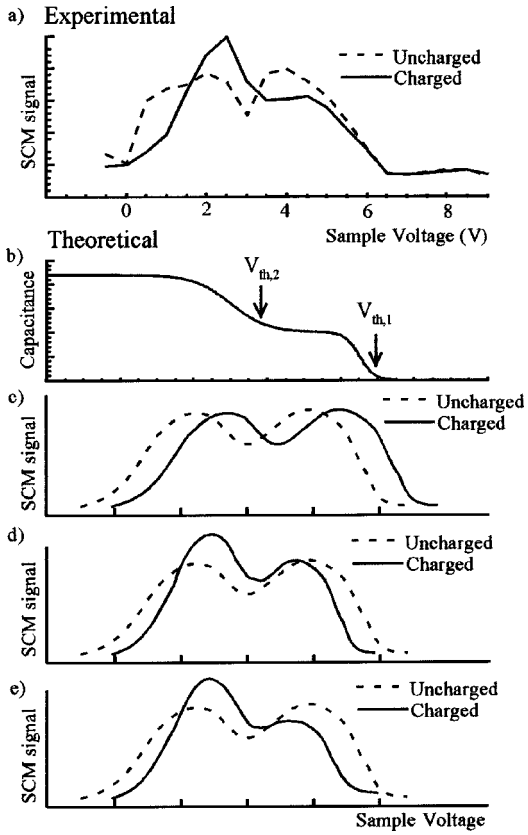

FIG. 4. (a) Measured SCM signal vs sample bias voltage for charged and uncharged sample regions derived from data in Fig. 3. (b) Schematic illustration of capacitance–voltage spectrum for a conducting probe tip and $Al_xGa_{1-x}N$/GaN HFET sample. (c)–(e) Schematic SCM signal spectra for charged (solid curves) and uncharged (dashed curves) regions of an $Al_xGa_{1-x}N$/GaN HFET sample structure for (c) positive trapped charge located at the $Al_xGa_{1-x}N$ surface; (d) positive trapped charge at the $Al_xGa_{1-x}N$ surface and negative trapped charge at or near the $Al_xGa_{1-x}N$/GaN interface; (e) positive trapped charge at the $Al_xGa_{1-x}N$ surface and within the GaN buffer layer and negative trapped charge at or near the $Al_xGa_{1-x}N$/GaN interface.

larger than that from the uncharged region until the sample bias voltage reaches 3–3.5 V. For sample bias voltages of ~3.5 V and above, the contrast reverts, qualitatively, to that observed at low sample bias voltages, with the SCM signals for the charged and uncharged regions gradually converging near zero for large positive sample bias voltages.

An analysis of the dependence of the SCM signal on bias voltage in the charged and uncharged regions can yield information about the possible locations of trap states that can become charged for large applied bias voltages. Figure 4(b) shows, schematically, a typical C–V characteristic for a conducting probe tip, insulating oxide layer, and n-$Al_xGa_{1-x}N$/GaN HFET epitaxial layer structure as a function of dc bias voltage applied to the sample.[11] For sample bias voltages $V > V_{th,1}$, the 2DEG at the $Al_xGa_{1-x}N$/GaN interface is depleted and the capacitance is small. For $V_{th,2} < V < V_{th,1}$, carriers accumulate at the $Al_xGa_{1-x}N$/GaN interface and the capacitance observed is essentially that of the $Al_xGa_{1-x}N$ barrier layer and the insulating oxide layer between the conducting tip and the sample surface. For $V < V_{th,2}$, carriers spill into the $Al_xGa_{1-x}N$ barrier and towards the $Al_xGa_{1-x}N$ surface, leading to an increase in capacitance. The SCM signal is related to the slope of the C–V curve, dC/dV, averaged over the ac modulation voltage amplitude.[23] The dashed lines in Figs. 4(c)–4(e) show, schematically, the resulting simulated SCM signal as a function of bias voltage for a typical $Al_xGa_{1-x}N$/GaN HFET sample structure.

To determine the locations of the traps, the effects of fixed charge layers in a variety of locations on the C–V characteristics of an $Al_{0.25}Ga_{0.75}N$/GaN HFET epitaxial layer structure were simulated using a one-dimensional Poisson/Schrödinger solver.[24] A layer of trapped positive charge at the surface will change the voltage at which the charge at the surface will be depleted and the depletion region will begin to extend into the sample, yielding a shift along the voltage axis in the C–V characteristics. The result is a constant shift in voltage in the C–V and the SCM signal curves, as shown schematically for a positive surface charge layer by the solid line in Fig. 4(c).

If in addition to trapped charge at the surface there is trapped charge at the $Al_xGa_{1-x}N$/GaN interface or within the $Al_xGa_{1-x}N$ barrier near the interface, the threshold voltage, $V_{th,1}$ may be shifted significantly, but there will be only a relatively small effect on the voltage $V_{th,2}$ at which spillover of electrons towards the $Al_xGa_{1-x}N$ surface occurs. Negative trapped charge at or near the heterojunction interface will partially compensate the positive polarization charge at the interface and thereby reduce the sheet carrier concentration in the 2DEG. As a result, the threshold voltage $V_{th,1}$ for the charged structure will shift to a lower sample bias voltage and the C–V and SCM signal characteristics near $V_{th,1}$ will change accordingly.

The effects of trapped negative charge at or near the interface will also significantly influence the C–V characteristics for $V_{th,1} < V < V_{th,2}$. As the depletion depth extends below the surface and approaches the interface for increasing sample bias, the voltage necessary to deplete the 2DEG at the interface will decrease, yielding a larger change in the depletion depth and therefore the capacitance for the same voltage change compared to that in the uncharged region. This larger change in the capacitance will cause the slope of the C–V characteristics and consequently the SCM signal in this region to increase, leading to the larger peak shown in Fig. 4(d) for the SCM signal near $V_{th,2}$ in the charged region.

Once the depletion depth extends below the $Al_xGa_{1-x}N$/GaN interface, the trapped charge in the vicinity of the heterojunction interface will lead simply to a constant shift in the voltage of the C–V characteristics. The SCM signal in this voltage range will then depend primarily on the charge carriers within the GaN, which we have assumed to be identical for the charged and uncharged regions. The change in the capacitance for positive bias voltages in this range will therefore be the same for both regions, yielding the same slope to the C–V characteristics. As shown in Fig. 4(d), the SCM signal peak near $V_{th,1}$ will therefore be of nearly identical height for both the charged and uncharged

regions, but will be shifted in voltage because of the difference in the surface and interface charge densities.

Figure 4(e) shows the result of adding positive trapped charge within the GaN layer below the 2DEG channel to the positive trapped surface charge and negative trapped heterojunction interface charge considered above. The positive charge in the GaN has little effect on the C–V characteristics until the depletion region extends below the interface; thus, the SCM signal for V well below $V_{\text{th},1}$ will not change significantly compared to that shown in Fig. 4(d). Once the depletion depth extends below the $Al_xGa_{1-x}N$/GaN interface, positive trapped charge in the GaN layer will reduce the change in depletion depth, and hence the change in capacitance, for a given change in voltage and thereby reduce the interface peak height of the SCM signal.

By comparing the experimental data illustrated in Fig. 4(a) with the simulations described above, several general trends are apparent. For $0\ \text{V} \leqslant V \leqslant 1.5\ \text{V}$, the shift between the charged and uncharged experimental curves in Fig. 4(a) suggests the presence of positive charge at the surface. The increased peak height in the SCM signal in the charged region near 2.5 V is expected for negative charge trapped at or near the $Al_xGa_{1-x}N$/GaN interface as described above. A possible mechanism for the generation of the surface and interface trapped charge is that the electrons are being forced from surface states into traps at or near the interface when large positive bias is applied. Finally, the reduced peak height near 5 V in the charged region suggests that positive charge is trapped within the GaN layer. Ionization of donorlike trap states and, hence an effective increase in n-type doping within the GaN during the charging process, can increase the amount of positive charge. Another possible factor is that negative charge at the interface will reduce the confinement of the 2DEG at the $Al_xGa_{1-x}N$/GaN interface, which allows the channel region to extend farther into the GaN layer. Such an extension of the channel region would also reduce the height of the SCM signal peak associated with depletion of the 2DEG. Finally, it should be noted that a certain amount of charging induced by the imaging process is expected in the uncharged region at large sample bias voltages, and that these effects will reduce the contrast between the charged and uncharged region. We believe that this effect is responsible for the convergence in the SCM signals observed in the charged and uncharged regions at sample bias voltages of $\sim$5–6 V.

IV. CONCLUSION

In conclusion, we have used scanning capacitance microscopy to characterize local charging and trap states in $Al_xGa_{1-x}N$/GaN HFET epitaxial layer structures. SCM imaging as a function of applied bias voltage enables electrostatic potential, charge, and mobile carrier distributions to be probed with submicron to nanometer-scale spatial resolution both laterally and in depth. Application of large dc bias voltages during imaging was found to lead to localized, long-lived sample charging analogous to charging of deep trap states in diodes, transistors, and other device structures under large applied bias. Bias-dependent SCM imaging of charged and uncharged regions of $Al_xGa_{1-x}N$/GaN HFET epitaxial layer structures combined with theoretical analysis and numerical simulations allows information about the nature and location of various trap states to be derived. Our studies indicate that positive charge is trapped at the $Al_xGa_{1-x}N$ surface and within the GaN buffer layer, while negative charge is trapped at or near the $Al_xGa_{1-x}N$/GaN heterojunction interface.

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