Gate leakage current mechanisms in AlGaN/GaN heterostructure field-effect transistors

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Gate leakage currents in AlGaN/GaN heterostructure field-effect transistor (HFET) structures with conventional and polarization-enhanced barriers have been studied. Comparisons of extensive gate leakage current measurements with two-dimensional simulations show that vertical tunneling is the dominant mechanism for gate leakage current in the standard-barrier HFET and that the enhanced-barrier structure suppresses this mechanism in order to achieve a reduced leakage current. An analytical model of vertical tunneling in a reverse-biased HFET gate-drain diode is developed to evaluate the plausibility of this conclusion. The model can be fit to the measured data, but suggests that additional leakage mechanisms such as lateral tunneling from the edge of the gate to the drain or defect-assisted tunneling also contribute to the total leakage current. The vertical tunneling current mechanism is shown to be more significant to the gate leakage current in III–V nitride HFETs than in HFETs fabricated in other III–V material systems, in which the lateral tunneling current component generally dominates the gate leakage current. © *2000 American Institute of Physics.* [S0021-8979(00)04523-0]

I. INTRODUCTION

Minimizing the off-state leakage current in III–V nitride heterostructure field-effect transistors (HFETs) is essential to their incorporation into circuits and systems in which low noise[1] and low power consumption are important considerations. One technique that has been used to reduce the gate leakage current in AlGaN/GaN HFETs exploits the strong polarization effects in the nitrides[2] to increase the HFET peak barrier height by including a GaN cap layer on top of the standard AlGaN barrier.[3] This strategy yielded a large reduction in gate leakage current compared to that in a conventional HFET without the GaN cap layer,[4] but it was unclear which leakage mechanisms were being suppressed in order to achieve the improved characteristics. The purpose of the current study is to determine the dominant current leakage paths in each structure and understand physically how the polarization-enhanced barrier structure reduces the gate leakage current. It was also anticipated that such a study might clarify some of the important aspects of gate leakage current mechanisms in nitride-based HFETs compared to HFETs fabricated in other material systems.

II. EXPERIMENTAL PROCEDURE

The epitaxial layer structures used in these studies were grown by low-pressure metalorganic vapor-phase epitaxy on *c*-plane (0001) sapphire substrates and employed an undoped 3 μm GaN layer for the channel. The conventional HFET structure consisted of a 300 Å undoped $Al_{0.25}Ga_{0.75}N$ layer deposited on the GaN channel layer as shown in Fig. 1(a). In the enhanced-barrier HFET structure, an undoped 225 Å $Al_{0.25}Ga_{0.75}N$ layer followed by an undoped 75 Å GaN layer were deposited on the GaN channel layer as shown in Fig. 1(b). The presence of a negative polarization sheet charge at the upper $Al_{0.25}Ga_{0.75}N$/GaN interface in the latter structure led to an increase in the peak barrier height in the HFET gate region from 1.52 eV for the conventional $Al_{0.25}Ga_{0.75}N$ barrier to 1.89 eV for the polarization-enhanced barrier structure.[3]

Transistors were fabricated using Ti/Al metallization annealed for 30 s at 950 °C for source and drain ohmic contacts and Ni/Au for Schottky gate contacts. The devices had gate lengths of 1 μm, gate widths of 25 and 50 μm, and a gate-drain spacing of 1 μm and were isolated by employing an ion implantation process with phosphorus and helium.[5] The gate current was measured as a function of gate-drain voltage both with fixed gate-source voltages and with the source floating in order to investigate the influence of the source on the leakage in the gate-drain diode.[6] Data were obtained for temperatures ranging from 175 to 500 K, as measurement of temperature-dependent current–voltage characteristics allowed a more detailed analysis of each leakage mechanism to be performed. Additionally, one- and two-dimensional numerical simulations were performed to estimate the magnitudes of the electric fields directly under the gate and at the drain-side edge of the gate contact. These simulations enabled a straightforward comparison of the two possible tunneling leakage paths illustrated in Fig. 2: vertical tunneling through the main gate area and lateral tunneling from the edge of the gate contact in each structure. Finally, an analytical expression was derived for vertical tunneling in a reverse-biased Schottky contact. This expression was then fitted to measured data to test the model and derive further information about the tunneling barrier in each structure.

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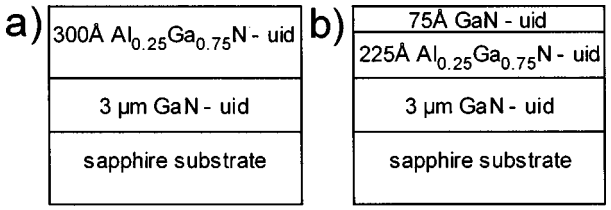

FIG. 1. Schematics of (a) the standard and (b) the enhanced-barrier AlGaN/GaN HFET layer structures indicating the doping concentration in the epitaxial layers as unintentionally doped (uid).

III. RESULTS AND DISCUSSION

Three main techniques were employed to analyze the gate leakage currents in the two structures under investigation: dc electrical characterization, numerical simulation, and analytical modeling. Both individually and in combination, these approaches provide extensive information concerning the nature and physical origin of gate leakage currents in the nitride HFET structures under investigation.

A. dc electrical characterization

Initial measurements of the gate-drain leakage current and breakdown voltages in both structures showed that the gate leakage current in the enhanced-barrier HFET (EB-HFET) was suppressed by over an order of magnitude compared to that in the standard-barrier HFET (SB-HFET).[4] Further measurements of the leakage current in the reverse-biased gate-drain diode as a function of temperature are shown in Fig. 3 for both structures. The source contact for these measurements was floating.

A number of features are worth noting in comparing the current–voltage ($I-V$) characteristics for the two structures. First, for reverse-bias gate-drain voltages V_{GD} below the threshold voltage ($-2.5\,\mathrm{V}<V_{GD}<0$), there is, for both structures, a rapid increase in current as the reverse-bias voltage is increased. As the bias for each device approaches the threshold voltage (approximately -2.5 V), however, the current begins to increase more slowly; for larger reverse-bias voltages the current depends only weakly on the reverse-bias voltage, especially in the case of the SB-HFET. The most likely explanation for this general behavior is that the leakage current is due to vertical tunneling through the main gate area, which is consistent with other studies of leakage current in AlGaN/GaN HFETs.[7] This can be understood by considering the potential within the HFET barrier as a function of gate-drain bias. As the diode is initially reverse biased, the two-dimensional electron gas in the channel begins to be depleted. In this voltage regime, the potential drop within the barrier increases substantially. Thus, for $-2.5\,\mathrm{V}<V_{GD}<0$, there is a significant change in the tunneling barrier, and it becomes much easier for electrons to tunnel from the metal gate contact into the semiconductor as the reverse-bias voltage is increased. Once the channel is fully depleted, the resistance between the gate and drain contacts increases and any additional voltage applied across the gate-drain diode is dropped primarily in the region between the gate and drain contacts. This was confirmed by two-dimensional numerical simulations as discussed below. Therefore, for this voltage regime, there is little change in the tunneling barrier and, consequently, only a slow increase in the leakage current due to vertical tunneling through the main gate area.

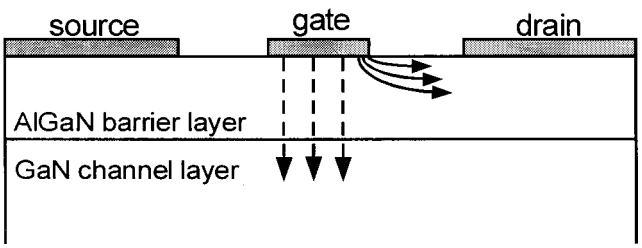

FIG. 2. Schematic of the HFET structure illustrating vertical (dashed lines) and lateral (solid lines) tunneling current leakage paths for the gate-drain diode.

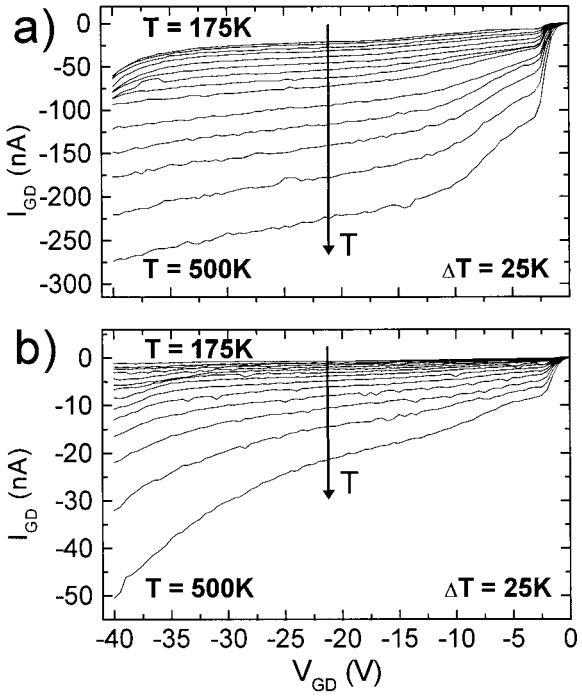

FIG. 3. Typical leakage current characteristics of the reverse-biased gate-drain diode for: (a) the standard and (b) the enhanced-barrier HFET structures as functions of temperature. Measurements are shown for $T=175-500$ K in steps of .25 K with the source contact floating.

Comparison of the $I-V$ characteristics of the two structures reveals that for reverse-bias voltages larger than approximately -2.5 V, the functional dependence of the gate current on gate-drain bias differs throughout the measured range of temperatures. At temperatures below ~350 K, the SB-HFET exhibits a linear increase in gate current with $-V_{GD}$ for $-30\,\mathrm{V}<V_{GD}<-4\,\mathrm{V}$ while for larger negative biases, the gate current increases more rapidly. This is in contrast to the EB-HFET which exhibits a linear increase in the gate current for the entire range of measured gate-drain voltages below $V_{GD}=-4$ V. The situation changes above ~350 K, when the SB-HFET gate current begins to show a linear dependence on gate-drain voltage for $-40\,\mathrm{V}<V_{GD}<-10\,\mathrm{V}$, and the gate current in the EB-HFET increases nonlinearly over the same voltage range. To explain the nonlinear behavior of the $I-V$ characteristics for the EB-HFET

in this voltage regime, it is necessary to consider another leakage mechanism. Lateral tunneling at the drain-side corner of the gate has been shown to be the dominant mechanism for gate-leakage current in other III–V HFETs[8] and, in devices in which lateral tunneling is important, the gate-drain current increases approximately exponentially with V_{GD}.[6] This suggests that in the voltage and temperature ranges where the gate current measured in our nitride HFET structures increases nonlinearly with $-V_{GD}$, lateral tunneling could be a significant contributing factor.

We have also computed the expected contribution to the leakage current from thermionic emission of electrons from the metal gate contact into the semiconductor and found it to be small compared to the measured values of the leakage current. This is due the large barrier heights of Schottky contacts on GaN and AlGaN, which make the thermionic emission leakage current negligible even for $T=500\,\mathrm{K}$. Other studies of the gate leakage current in AlGaN/GaN HFETs included the thermionic emission contribution to the current density and concluded that electron tunneling from the gate metal into the semiconductor is the dominant leakage mechanism.[7] Therefore, the thermionic emission mechanism will be neglected for the remainder of the analysis.

Based on the above measurement and analysis, we may conclude that: (1) vertical tunneling through the main gate area is the most important leakage mechanism and (2) lateral tunneling becomes non-negligible in certain temperature and voltage ranges. It is next desirable to obtain a better understanding of the lateral tunneling and how it contributes to the total gate leakage current. Studies of HFETs in other III–V material systems have shown that the bias applied to the source contact can have a significant effect on the lateral tunneling in the gate-drain diode if lateral tunneling is the dominant leakage mechanism.[6,9,10] However, if the gate-source bias (V_{GS}) changes the vertical tunneling barrier, the leakage current should also be affected in a device where vertical tunneling dominates. Thus, gate-leakage current measurements as a function of V_{GS} are not sufficient to determine the leakage path without a more detailed understanding of how the gate-source bias affects the vertical and lateral electric fields in the device which influence, respectively, the vertical and lateral tunneling current components. The strategy employed in our work was, therefore, to measure the gate leakage current as the gate-source bias was varied and to perform two-dimensional simulations to elucidate the effect of V_{GS} on the vertical and lateral electric fields. Careful analysis of the results of these two investigations then enables an accurate determination of the leakage paths in both device structures and consequently yields a better understanding of the effect of the enhanced barrier.

Measurements of the gate current as a function of gate-drain and gate-source bias were performed at room temperature for both structures. As the gate-source reverse-bias voltage is increased, current flows from the gate to the source, so it is necessary to subtract this current component from the measured gate current in order to compare the gate-drain leakage for different values of V_{GS}. For $V_{GD}=0\,\mathrm{V}$, the gate-source current I_{GS} is the only contribution to the measured gate current, and I_{GS} for all gate-drain biases was estimated as the measured current with $V_{GD}=0\,\mathrm{V}$. Although V_{GD} could affect I_{GS},[6] the gate-source current is small compared to the gate-drain current for the values of V_{GS} used, and the error from this estimate should not significantly affect the resulting value for the gate-drain current. Figure 4 shows the increase in gate-drain leakage current for each value of V_{GS} compared to that for $V_{GS}=1\,\mathrm{V}$ with the source current appropriately subtracted. It is apparent from Fig. 4 that the gate-source voltage has a large effect on the SB-HFET gate-drain leakage, whereas V_{GS} does not significantly influence the gate-drain leakage in the EB-HFET. Such a clear difference in the behavior of the two device structures makes this an important observation, and the result will be utilized later in drawing conclusions about the differences in gate leakage current mechanisms between the two device structures.

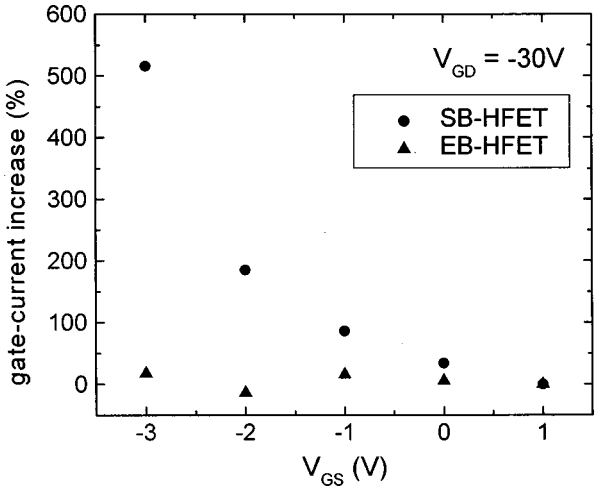

FIG. 4. Measured increase in gate current as a function of gate-source voltage normalized to the gate current measured at $V_{GS}=1\,\mathrm{V}$ for the standard- and enhanced-barrier HFETs with $V_{GD}=-30\,\mathrm{V}$.

B. Numerical simulation

As stated earlier, simulations of the vertical and lateral electric fields in each device are an important component in determining the leakage paths. Using Medici,[11] two-dimensional simulations of both structures were performed for $-40\,\mathrm{V}<V_{GD}<0\,\mathrm{V}$ and $-6\,\mathrm{V}<V_{GS}<0\,\mathrm{V}$. A background n-type dopant concentration of $1\times10^{17}\,\mathrm{cm}^{-3}$ was assumed for the bulk GaN in the simulations. The value for the n-type dopant concentration in the AlGaN barrier layer was assumed to be $2\times10^{18}\,\mathrm{cm}^{-3}$ in each device, and the GaN cap layer of the EB-HFET was taken to have an n-type dopant concentration of $5\times10^{17}\,\mathrm{cm}^{-3}$. Fixed polarization charges were incorporated into the simulation by placing heavily doped, 10 Å layers next to the interface where the polarization charges would be located in the heterostructure. The three-dimensional dopant concentration was chosen such that, when multiplied by 10 Å, the equivalent of the theoretically predicted interface charge[12] was achieved.

The threshold voltages of the simulated structures were adjusted to match the measured threshold voltages of approximately $-2.5\,\mathrm{V}$ by including a p-type GaN buffer layer 100 Å below the n-type GaN channel layer. This buffer layer

TABLE I. Simulated electric field component magnitudes in the standard- and enhanced-barrier HFET structures for gate-source biases of 0 and −6 V and a gate-drain bias of −40 V.

V_{GS} (V)	Electric field component	Electric field (MV/cm)	
		SB-HFET	EB-HFET
0	vertical	−1.06	−0.90
0	lateral	−0.12	−2.45
−6	vertical	−2.05	−0.90
−6	lateral	−1.75	−2.45

was necessary to correctly simulate the pinch-off characteristics of the device because adjusting the interface charges in the structures would have required a large deviation from the predicted values of the polarization charge and, therefore, altered the electric fields which were being investigated. The vertical electric field was taken as the value of the vertical component of the electric field at the metal–semiconductor interface under the middle of the gate, and the lateral electric field was taken as the maximum value of the lateral component of the electric field 25 Å below the semiconductor surface near the drain-side corner of the gate.[9] All simulations were performed for devices operating at 300 K.

Simulations of the device structures as a function of gate-drain bias showed that the vertical fields varied only slightly with gate-drain reverse bias once the threshold voltage was exceeded. This result is consistent with the previously proposed explanation for the dependence of the gate current on gate-drain voltage, which was based on vertical tunneling being the dominant mechanism. In contrast to the behavior observed for the vertical electric field, simulations showed, as expected, that the lateral electric field increased significantly as the gate-drain bias was increased. Therefore, simulations of the electric fields for varying gate-drain bias are consistent with the expected behavior and support the earlier conclusion based on the analysis of the $I_{GD}-V_{GD}$ characteristics that vertical tunneling is significant in these structures.

Simulations of the vertical and lateral electric fields for varying gate-source voltages provide a more detailed understanding of the interplay between vertical and lateral tunneling in each device structure. These simulations reveal an important difference between the SB-HFET and EB-HFET and help explain the observed electrical characteristics. In the SB-HFET structure, both the vertical and lateral electric fields are significantly influenced by the variation in gate-source voltage. Table I shows the magnitudes of the vertical and lateral electric field components predicted by our simulations for $V_{GS}=0$ V and −6 V with $V_{GD}=-40$ V. The data in Table I reveal that when V_{GS} is increased from 0 to −6 V in the SB-HFET, the vertical electric field increases by a factor of 2, and the lateral electric field increases by an order of magnitude. In contrast, the vertical and lateral electric fields in the EB-HFET structure show virtually no dependence on the gate-source voltage. Thus, the dramatically different characteristics of the SB-HFET and EB-HFET shown in Fig. 4 can be understood in terms of the dependence of the vertical and lateral electric fields in the device on V_{GS}, or lack thereof. The clearly observed sensitivity of the SB-HFET gate leakage current to V_{GS} arises because of the strong dependence of the electric fields and, consequently, of the tunneling currents on V_{GS}. In contrast, the observation that the EB-HFET gate leakage is independent of V_{GS} can be explained by the fact that the electric fields remain approximately constant as V_{GS} is varied.

The most likely physical explanation for the contrasting behavior of these device structures is based on the idea that the variation of the lateral depletion of the semiconductor between the gate and source affects the charge distribution on the gate electrode and thereby influences the electric field around the gate.[6] Simulations of the depletion regions in each device for different gate-drain and gate-source biases showed that as the gate-drain bias was increased in each device, the lateral depletion edge on the source side of the gate moved closer to the edge of the gate electrode. In the case of the EB-HFET, the depletion edge moved toward the gate electrode faster than in the SB-HFET because of the lower dopant concentration in the GaN cap layer compared to that in the AlGaN barrier of the SB-HFET. For gate-drain reverse-bias voltages greater than −5 V, the lateral depletion edge in the GaN cap layer of the EB-HFET is located at the edge of the gate electrode regardless of gate-source bias. Conversely, the lateral depletion edge in the SB-HFET barrier layer is still located between the gate and source electrode and varies with gate-source bias. Thus, in the case of the SB-HFET, the lateral depletion between the gate and source which is dependent on the gate-source bias can affect the electric field around the gate for the entire range of gate-drain biases. In the EB-HFET, however, the gate-source bias does not influence the electric field for gate-drain reverse-bias voltages greater than −5 V because the lateral depletion edge has been pulled to the edge of the gate electrode by the gate-drain bias and can no longer be affected by V_{GS}.

Simulations also provide insight into the dominant leakage path in each device. The relative sizes of the vertical and lateral electric fields in each device can suggest which mechanism contributes more significantly to the total leakage. Throughout the range of simulated bias voltages, the vertical electric field in the EB-HFET is consistently lower than that in the SB-HFET. Conversely, the lateral electric field in the EB-HFET is always higher than that in the SB-HFET. Since the leakage current in the SB-HFET is higher than that in the EB-HFET, these observations suggest that vertical tunneling is the dominant leakage mechanism in the SB-HFET. This conclusion is consistent with the strong dependence of the gate leakage current on gate-source bias in the SB-HFET because simulations showed that the vertical electric field varied with V_{GS} for this structure. In the EB-HFET, the vertical electric field is greater than the lateral electric field for small gate-drain biases, but as V_{GD} is increased, the lateral electric field becomes greater than the vertical electric field. Thus, vertical tunneling dominates for small V_{GD} and lateral tunneling begins to contribute as V_{GD} is increased. This confirms the explanation that was proposed when considering the shape of the gate current versus gate-drain bias curves shown in Fig. 3.

The physical explanation for the different characteristics of the SB-HFET and EB-HFET is understandable in terms of the device parameters that affect tunneling in an HFET. The vertical electric field is influenced by the dopant concentration and the Schottky barrier height of the semiconductor in contact with the gate metal. In the SB-HFET, the gate contact is made to $Al_{0.25}Ga_{0.75}N$ which has a higher background doping concentration and a higher Schottky barrier than the top layer of the EB-HFET, which consists of GaN. The effective barrier enhancement due to the polarization charges in the EB-HFET is not present when the gate-drain diode is strongly reverse biased and, therefore, the height of the barrier for electrons tunneling from the metal into the semiconductor is determined primarily by the Schottky barrier height. Thus, the lower barrier and background doping concentration in the EB-HFET lead to a smaller vertical electric field than is present in the SB-HFET. Although the higher Schottky barrier in the SB-HFET increases the vertical electric field, the higher barrier also decreases the probability that electrons will tunnel from the metal into the semiconductor. Therefore, it is possible that another mechanism is partly responsible for the increased vertical tunneling in the SB-HFET compared to the EB-HFET. One possible explanation for the larger amount of vertical tunneling that we believe occurs in the SB-HFET is that the GaN cap layer of the EB-HFET improves the structural integrity of the material and decreases defect-assisted tunneling.[13] Both the lower electric field and the lower probability for defect-assisted tunneling in the EB-HFET are viable explanations for the decreased vertical tunneling in this structure.

In other III–V HFETs it is believed that lateral tunneling is the dominant mechanism,[6–10] so it is important to understand why the nitride-based transistors in this study appear to behave differently. The lateral electric fields in InAlAs/InGaAs and AlGaAs/InGaAs HFETs predicted by Somerville and del Alamo[9] using simulations and an analytical model are comparable to those obtained from the simulations performed in this investigation. To estimate the vertical electric field in other III–V HFETs, one-dimensional simulations of an $Al_{0.25}Ga_{0.75}As$/GaAs HFET were performed.[14] The vertical electric field in such a device was approximately an order of magnitude smaller than the vertical electric fields predicted by simulations of the nitride-based HFETs. The difference in vertical fields arises because of the higher effective doping concentration due to the high concentration of defects in the nitrides[15] and the large Schottky barrier height inherent to the higher-band-gap nitride HFETs. Defect-assisted tunneling can also contribute significantly to the vertical tunneling in metal–nitride contacts.[13] Therefore, despite the significantly larger Schottky barrier height, it is not unreasonable to expect that vertical tunneling will be more significant in nitride-based HFETs than in conventional III–V HFETs and that lateral tunneling will be comparable in both types of devices.

C. Analytical modeling

To further understand how vertical tunneling occurs in the SB-HFET and EB-HFET device structures, an analytical model of the tunneling through a reverse-biased Schottky diode was developed. Fitting the analytical model to measured leakage currents can enable information about the tunneling barrier to be extracted. This information can then be compared to the physical parameters of the semiconductor to determine the degree to which vertical tunneling is the dominant mechanism in the SB-HFET and a significant part of the leakage current in the EB-HFET.

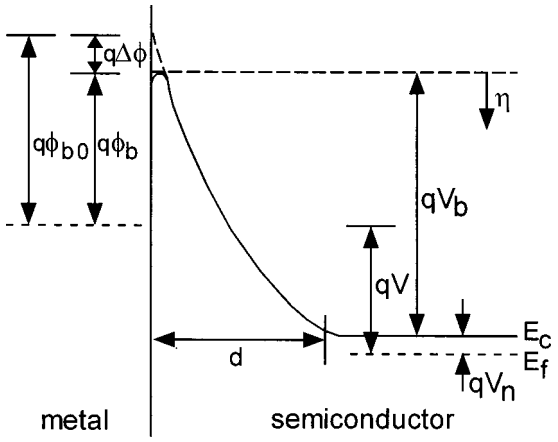

FIG. 5. Conduction band diagram of a metal–semiconductor Schottky gate contact showing parameters used in the derivation of the analytic model of vertical tunneling in a reverse-biased gate-drain diode.

The analytical model formulated for this study was adapted from an analysis[16] of the tunneling in a forward-biased metal–GaN Schottky diode which considered the current density due to tunneling of electrons from the semiconductor into the metal $J_{s\rightarrow m}$. Since this current is small in reverse bias, the model was extended in our work to account for electrons tunneling from the metal into the semiconductor. The resulting current density $J_{m\rightarrow s}$ is the important contribution to current flow in a reverse-biased metal–semiconductor junction. In the derivation, the barrier is assumed to be composed of only one material so the heterojunctions in the devices are neglected. The GaN cap layer in the EB-HFET may affect the results of the analysis, and this issue will be discussed later.

Figure 5 shows a schematic conduction band diagram for the reverse-biased metal–semiconductor junction and defines relevant parameters used in the derivation of the gate leakage current. The basic equation describing current flow due to tunneling of electrons from the metal into the semiconductor is

$$J_{m\rightarrow s}=\frac{A^{*}T}{k}\int_{0}^{qV_b}F_m T(\eta)(1-F_s)\,d\eta, \tag{1}$$

where A^{*} is the effective Richardson's constant, k is Boltzmann's constant, F_m is the Fermi–Dirac distribution function in the metal, F_s is the Fermi–Dirac distribution function in the semiconductor, qV_b and η are energies defined in Fig. 5, and $T(\eta)$ is the quantum transmission coefficient of the electrons through the approximately triangular Schottky barrier, given by

$$T(\eta)=\exp\left(-\frac{4}{3}\frac{\sqrt{2m^*}}{\hbar}w\sqrt{\eta}\right). \tag{2}$$

The parameter w in Eq. (2) is the width of the tunneling barrier and can be expressed as

$$w(\eta)=\frac{\eta}{qV_b}d=\frac{\eta}{qV_b}\sqrt{\frac{2\varepsilon_s}{qN_d}}\sqrt{V_b}, \tag{3}$$

where d is the distance that electrons must tunnel at the base of the triangular barrier as shown in Fig. 5. The energy dependence of the barrier width must be accounted for in this derivation because electrons in the metal may tunnel through the barrier throughout the range of energies encompassed by the integral in Eq. (1). This is in contrast to the derivation for the tunneling of electrons from the semiconductor into the metal since no simplifying assumption can be made about the energy at which the majority of the tunneling occurs. In this case the expression for the tunneling probability can be simplified to

$$T(\eta)=\exp\left(-\frac{\eta^{3/2}}{\sqrt{qV_b}}\frac{8}{3}\sqrt{\frac{m^*\varepsilon_s}{N_d}}\frac{1}{q\hbar}\right)=\exp\left(-\frac{\eta^{3/2}}{E_{00}\sqrt{qV_b}}\right), \tag{4}$$

where

$$E_{00}=\left(\frac{8}{3}\sqrt{\frac{m^*\varepsilon_s}{N_d}}\frac{1}{q\hbar}\right)^{-1}. \tag{5}$$

A final simplifying assumption can be made about the occupation of states in the semiconductor conduction band since very few of the electrons tunneling from the metal into the semiconductor will tunnel at the base of the barrier, where most of the electrons in the conduction band are located. It can therefore be assumed that the states in the conduction band of the semiconductor are unoccupied, yielding $(1-F_s)\approx 1$. An effective mass of $0.2m_0$ was used in the calculations,[17] and the effective Richardson's constant used in Eq. (1) was based on this value. Smaller values for A^* have been observed experimentally,[16] but using such values would not affect the conclusions drawn from the calculations.

The resulting expression for the current density cannot be integrated analytically, so the results described below were obtained by computing the integral in Eq. (1) numerically. This made the fitting procedure considerably more difficult since there are three variables that can be adjusted in the equation for the leakage current—V_b, N_d, and ϕ_b. However, the first of these is related to the applied bias so it was possible to estimate its value independent of the fitting procedure. To do this, one must first note that the voltage drop between the gate and drain contacts occurs primarily in two locations: vertically along the structure as qV labeled in Fig. 5, and laterally across the resistance connecting the gate and drain. By simulating the vertical voltage drop in the structure as a function of bias applied between the gate and drain contacts, the fitting parameter V_b could then be estimated accurately from the expression

$$qV_b=q\phi_b-qV_n-qV, \tag{6}$$

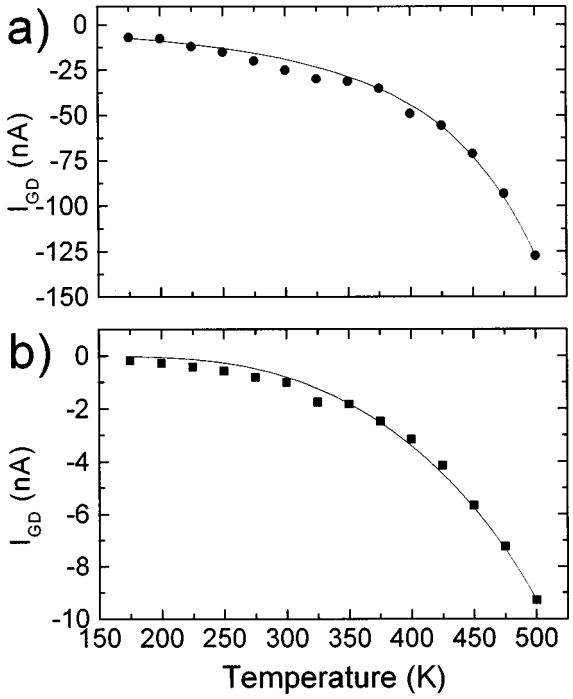

FIG. 6. Measured (squares) and calculated (curves) gate currents as a function of temperature in a gate-drain diode biased at $V_{GD}=-5$ V and with the source floating for: (a) the standard and (b) the enhanced-barrier HFET structures.

where qV_n is distance between the conduction band edge and the Fermi level in the semiconductor, E_c-E_f, as shown in Fig. 5. If there were no lateral voltage drop, qV would be equal to the applied gate-drain bias voltage.

With these assumptions, the two independent fitting parameters are N_d and ϕ_b. To fit the measured data, a physically reasonable value for one parameter was chosen and the other variable was adjusted to match the measured data at one current–temperature data point. The integral expression was then evaluated over the range of temperatures for which data were available, and the resulting curve was compared to the measured data. Different combinations of N_d and ϕ_b that yielded the same current from the analytical expression as the measured value for the selected temperature were then used to generate theoretical curves which were compared to the measured data. With this procedure, a unique combination of values for N_d and ϕ_b could be found that matched the measured data for the entire temperature range.

Figure 6 shows plots of the measured and calculated gate current as a function of temperature for each device. The experimental data shown were obtained for $V_{GD}=-5$ V with the source floating. This gate-drain bias was chosen because the lateral electric fields in each device should have been low enough that vertical tunneling, as opposed to lateral tunneling, would be the dominant leakage mechanism. Simulations showed that an applied bias of -5 V between the gate and drain corresponded to a value of approximately -3 V for V as defined in Fig. 5. The values of N_d and ϕ_b that provided the best fit of the analytical expression to the measured data are given in Table II.

It is clear from Fig. 6 that the calculated curves fit the

TABLE II. Barrier layer doping density, N_d and barrier height ϕ_b obtained by fitting the analytical expression derived for vertical tunneling to the measured data for the standard and the enhanced-barrier HFETs.

Device structure	N_d (10^{19} cm^{-3})	ϕ_b (eV)
SB-HFET	1.4	1.23
EB-HFET	1.5	1.55

measured data very well, but the values for N_d that are derived from this procedure are unreasonably high. High donor concentrations in the semiconductor would lead to a thinner tunneling barrier and, therefore, more tunneling current. Thus, additional leakage mechanisms besides tunneling must contribute to the total gate leakage current in these device structures. In the actual device structures tested, it is possible, and probably quite likely, that defect-assisted tunneling contributes an additional leakage current mechanism.[13] This would explain the higher calculated values of N_d since the model does not include this mechanism. Defect assisted tunneling could also cause the SB-HFET barrier height ϕ_b to seem lower than its expected Schottky barrier height of 1.52 eV in this analysis since a lower barrier would increase the probability that electrons will tunnel from the metal into the semiconductor. The value of ϕ_b obtained for the EB-HFET is higher than the expected value of the Schottky barrier height of the Ni/Au–GaN contact which is approximately 1 eV.[18] The explanation for this anomalous value is less clear, but the polarization effects and band offset at the top GaN/AlGaN interface which were neglected in the derivation of the tunneling current could be responsible for making the conduction band edge higher in reverse bias than simulations suggested. This effect would make the barrier seem higher and yield a greater barrier height than expected.

The values of N_d and ϕ_b obtained by fitting the data in this manner for $V_{GD}=-5$ V should also fit the data for higher gate-drain biases if the parameter qV_b in the analytical expression is increased to account for the larger voltage drop across the structure. The increase in qV_b will not be very large since most of the applied voltage for gate-drain bias voltages beyond -5 V is dropped across the gate-drain resistance. This technique worked well for the SB-HFET, but higher gate-drain biases could not be fit for the EB-HFET with this model even with different values for N_d and ϕ_b. This suggests that vertical tunneling remains the dominant mechanism in the SB-HFET even when the gate-drain bias is increased, whereas another leakage mechanism becomes important in the EB-HFET for higher gate-drain biases. Consistent with conclusions drawn earlier in this study, lateral tunneling is the most likely mechanism that increases to a significant level as V_{GD} is increased in the EB-HFET because the lateral electric field is increasing.

IV. SUMMARY

An investigation of gate leakage current mechanisms in AlGaN/GaN HFET structures with a conventional AlGaN barrier and a polarization-enhanced GaN/AlGaN barrier has been conducted using a combination of dc electrical measurements, numerical simulations, and theoretical analysis. Extensive incorporation of two-dimensional computer simulations of the electric fields in the devices and an analytical model of vertical tunneling through the barrier layer of a reverse-biased HFET gate-drain diode into the investigation was essential in elucidating the relevant leakage current mechanisms in each structure. Careful comparison of gate-drain leakage-current measurements as a function of gate-source voltage with simulated electric fields showed that vertical tunneling is the dominant mechanism in the SB-HFET and both vertical and lateral tunneling are important in the EB-HFET. Theoretical modeling of the vertical tunneling in each device confirmed that lateral tunneling becomes non-negligible in the EB-HFET as the gate-drain bias is increased and showed that an additional leakage mechanism such as defect-assisted tunneling must be present in both structures to account for the measured leakage currents, which were slightly larger than expected from the analytical model. This work has confirmed the importance of the vertical tunneling current component to the gate leakage current in III–V nitride HFETs and has further shown that additional leakage current mechanisms such as lateral tunneling and defect-assisted tunneling contribute to the total gate leakage current. Based on our observations, the vertical tunneling mechanism should be substantially more significant to the gate leakage current in nitride-based HFETs compared to that in HFETs fabricated in other III–V material systems.

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